Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. SUN-P5403	Serial No. 09/982,452
Information Disclosure Statement by Applicant	Applicant: Manjunath D. Harista	
(Use several sheets if necessary)	Filed: October 17, 2001	Group: 2825

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
BT	A	5,644,498	7/1/97	Joly et al.			1/25/1995
	B	5,963,729	10/5/99	Aji et al.			6/26/1997
	C	6,289,412	9/11/01	Yuan et al.			3/12/1999
	D	5,778,216	7/7/98	Venkatesh			7/7/1998
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	F	5,974,245	10/26/99	Li et al.			5/30/1997
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Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No
BT	P	WO 95/34036	12/14/95	WO			X	

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BT	Q	R.B. Mueller et al., "Parallel Switch-Level Simulation for VLSI", IEEE, 1991, pp. 324-328
	U	Scot Boon et al., "High Performance Clock Distribution for CMOS Asics", IEEE 1989, pp. 15.4.1 - 15.4.5
	V	H. Fair et al., "XP-000862228 SP 25.2: Clocking Design and Analysis for a 600MHz Alpha Microprocessor", IEEE International Solid-State Circuits Conference, 1998, pp. 389-399 & 473
	W	International Search Report, PCT/US 02/32937, International filing date October 15, 2002, date Search Report mailed January 28, 2004.
	X	B. Lamson et al., "A Processor for a High-Performance Personal Computer, Seventh Annual Symposium on Computer Architecture, pp. 146-160, May 1980.
	Y	C-S Wu et al., "An Automatic Cell Characterization Environment for Cell-Based Design Methodology", IEEE pp. 326-329, May 1993
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	AA	U-S Yim et al., "A Floorplan-based Planning Methodology for Power and Clock Distribution in ASICs:, Proceedings ACM/IEEE Conference on Design Automation, pp. 766-771, June 1999.
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Examiner	Date Considered
	08/16/04

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.